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A Novel Dynamic Voltage Restorer with Cascaded H-Bridge Inverter

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ABSTRACT: In this paper proposes the mitigation of the voltage sag occurring in the photovoltaic system using Dynamic Voltage Restorer (DVR) has been presented. Simulation results of Photo Voltaic system (PV), Dynamic Voltage Restorer (DVR) and local grid are presented. This study presents design and analysis of a DVR which employs a cascaded multilevel inverter with capacitors as energy sources. Controlling the voltage of capacitors around a reference voltage and keeping the balance between them, in standby and compensation period, is one of them. This paper analyze the performance of a DVR with multilevel inverter, using minimum required numbers of switches to compensate voltage sag and swell to regulate the load voltage to the best possible extent. To mitigate the voltage sags as fast as possible a fast three-phase estimation method is employed to minimize the delay of DVR. By using simulation results we can analyze the proposed method and also performance of the control scheme.

KEYWORDS: DC-DC converter, multilevel inverter, FACT device.

I.INTRODUCTION

The solar power generation systems are getting more attention because solar energy is abundantly available, more efficient and more environmental friendly as compared to the conventional power generation systems such as fossil fuel, coal or nuclear energy. The most common PQ problem that both industrial and commercial consumers suffer from is voltage sag [3, 4].

Voltage sags usually originate from several sources, including faults on facility side or the utility network, reclosing the circuit breakers, and in-rush current of large electrical motors at startup. As a flexible AC transmission system (FACTS) device, dynamic voltage restorer (DVR) is employed for mitigation of voltage sags through series injection of voltage and restoring the dropped supply voltage to its normal level [5, 6]. Generally a DVR is made of four main units: measurement stage, control unit, voltage source inverter and series injection transformer; the latter one is a bulky low-frequency transformer which increases the system cost. Since the inverter is of 2-level conventional type, its switching frequency has to be as high as 10 kHz and a filter is needed at the output side.

The proposed DVR system does not need any energy storage, since it draws the energy required for voltage compensation from the grid. While this topology benefits from the advantages of eliminating
energy storage system, such as smaller size and lower costs, it has some negative impacts on supply network currents: the supply currents will increase during compensation and the switching distortions will be fed to the line currents. It uses a boost converter to mitigate voltage sags and a buck
converter in case of voltage swells. Due to single stage power conversion, size of the energy storage was reduced.
The objective of this paper includes
1. To mitigate the voltage hang down
2. Effective usage of the renewable energy resources.
3. To compensate for the voltage disturbance using Dynamic Voltage Restorer (DVR)

It is a compact, cost effective and reliable DVR with a simple control system. Regarding the topology that uses only two switches, this DVR requires high switching frequency, as high as 6 kHz, and an output low-pass filter.

A medium voltage DVR with cascaded H-bridge (CHB) converter has been introduced [6]. This DVR employs multiple DQ transforms to implement its measurement and control strategy. The multiple DQ transform system allows fast and accurate operation of the DVR under harmonics and unbalanced conditions. The DC–DC

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converter allows for changing the DC link voltage so output voltage of the converter has the maximum possible number of levels for a wide range of voltage sags. Since the output voltage is always a well-shaped multilevel voltage, this DVR needs a very small output filter, but the extra DC–DC converter increases the power losses and system cost.

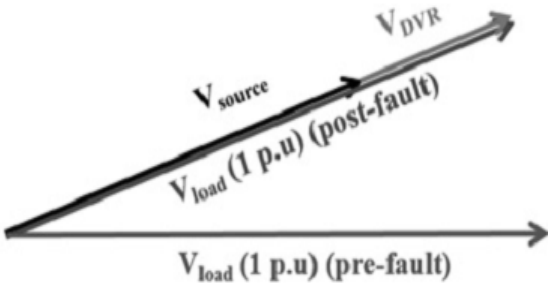
In this paper, the recorded data for the MWPI [2] is used as the base data for design of CHB-based DVR A fast estimation method for unbalanced three-phase voltage systems, which is able to estimate magnitude and phase of three-phase voltage/currents with maximum delay of half a cycle.

II. VOLTAGE RESTORATION AND THE MULTILEVEL CONVERTER

2.1 Zero Energy Voltage Restoration

As a FACTS device, DVR is installed in series with supply lines of industrial plants. Therefore, in case of voltage sag, it can inject a voltage in series with the supply voltage, restoring it to the nominal value. The compensation is possible in three different ways: post-fault, pre-fault and zero energy compensation [5].

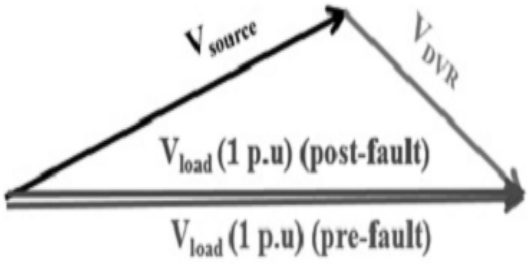
Fig. 1 displays corresponding phasor diagrams of these methods. In post-fault mode, depicted in Fig. 1a, the injection voltage is in-phase with the source voltage, where the amplitude of load voltage is kept constant.



(a)

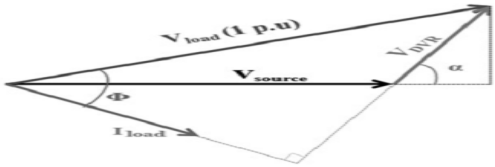
This technique is the simplest way of compensation with the smallest amount of injection voltage, while it requires the largest amount of active power. In order to perform post-fault compensation, the measurement unit determines depth of voltage sag and phase of the source voltage. This signal is fed to the inverter and the compensating voltage is generated based on it.

The compensation voltage will be added to the source voltage and restore the load voltage to nominal value.



(b)

Fig. 1 illustrates pre-fault compensation. This method is employed for protection of loads that are sensitive to phase-jump. In this method, the injection voltage is calculated in a way that not only the magnitude of load voltage is restored to the nominal value, but also its phase is restored to the initial value prior to voltage sag. The method which is employed in this research is zero energy compensation, displayed in Fig. 1c.



(c)

Fig.1 Different compensation techniques
a. Post-fault b.Pre-fault c.Zero energy approach.

Φ is the load angle, and α is the phase difference between network and DVR voltage. Phasor of DVR voltage (VDVR) is perpendicular to load current (I load)

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In this mode, the compensation voltage is injected in a way that to be orthogonal to Voltage restoration and the multilevel converter 2.1 Zero energy voltage restoration As a FACTS device, DVR is installed in series with supply lines of industrial plants. Therefore, in case of voltage sag, it can inject a voltage in series with the supply voltage, restoring it to the nominal value. The compensation is possible in three different ways: post-fault, pre-fault and zero energy compensation [5].

In order to perform post-fault compensation, the measurement unit determines depth of voltage sag and phase of the source voltage. On the basis of this data, the control system will then generate a reference sinusoidal signal which is in-phase with the source voltage and its magnitude is equal to depth of voltage sag. Therefore, active power is not transferred between the DVR and the load. This method is usually adopted for protection of high power loads.

The estimation unit of a DVR continuously measures the source voltage of the plant and generates a signal as soon as it drops below 90% of nominal value. In zero energy compensation, the voltage of DC-link capacitors will not drop during compensation. According to the phasor diagram of zero energy compensation in Fig.1c, the following equations are derived, where Vload is assumed to be 1pu and is not written in the following equation

$$cos^2\emptyset + (sin\emptyset - V\_DVR)^2 = V_{source}^2 \qquad (1)$$

$$(V_{source} + V_{DVR}.cos\alpha)^2 + (V_{DVR}.sin\alpha)^2 = 1 \qquad (2)$$

where VDVR and Vsource are the magnitudes of the injection voltage and the source voltage, respectively. α is the phase difference between their phasors and Φ is the phase difference between the load voltage and load current. Considering (1), it can be concluded that

$$\lceil (V_{DVR}\rceil = \left|\sqrt{|V_{source}^2 - cos^2\emptyset|} - sin\emptyset\right| \qquad (3)$$

Magnitude of injection voltage (VDVR) can be calculated through (3).

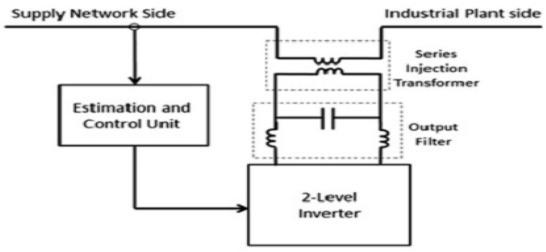
Yet α should be determined for the zero energy compensation approach (phase of VDVR) and then generated by inverter. α is calculated from (2) as follows

$$cos\alpha = \frac{1 - V_{source}^2 - V_{DVR}^2}{2V_{source}V_{DVR}} \qquad (4)$$

Hence, three phase locked loops (PLLs) are needed in this scheme. Two PLLs for calculating phase of load voltage and load current; where the difference between them gives the load angle (Φ). The third one estimates phase of the supply voltage, which is considered as phase reference in phasor calculation.

2.2 Benefits And Challenges Of The Multilevel Converters

A DVR with conventional converter is displayed in Fig. 2a. In addition to the converter, estimation unit, and control stage, the system has a series injection transformer, bypass thyristors and output filters. The two anti-parallel thyristors bypass the DVR terminals when the supply voltage is in normal range to prevent the losses at the DVR and to protect it against the electrical faults.



(a)

Depending on the compensation method, 10–20% of nominal load power may pass through this transformer during compensation. Assuming there is a power source that could provide this level of power, the transformer would be a bulky element which adds losses to the system.

Fig. 2b illustrates structure of the DVR that is utilized in this paper. This DVR employs a multilevel CHB converter. This type of converter is extremely modular and generates voltage waveforms with small dv/dt and low total

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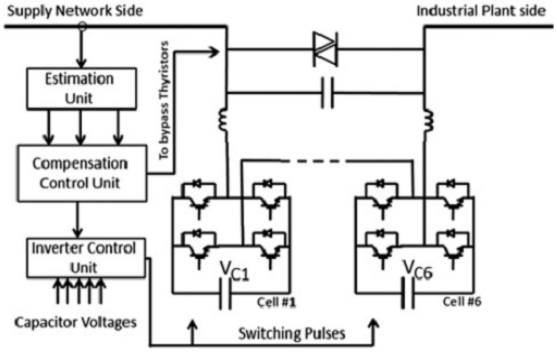
harmonic distortion (THD). Moreover, due to series connection of H-bridge cells, it can be easily extended for different voltage and power levels and one can perform fault-tolerant algorithms during the failure of power switches.



(b)

Fig. 2 DVR structures a) Conventional DVR b) CHB-based DVR

A CHB converter with n H-bridge cells is able to synthesize 2n + 1 levels at its AC terminals. Due to the synthesized multilevel waveform, the CHB converter needs a small filter on its output terminals to keep the THD within acceptable range [17]. The reduction in size of the output filter leads to lower losses and system costs.

Table 1
Voltage sags recorded in MWPI

No.	Sag depth,%	Sag duration, ms
1	12.4	40
2	12.4	50
3	13.2	60
4	11.1	50
5	11.2	30
6	19.1	50
7	16.9	70
8	11.4	350
9	42.4	60

Table 1 lists details of the voltage sags. It can be seen that the depth of voltage sags are between 10 and 20% of nominal value for eight (out of nine) events.

III. CONTROLLING AND BALANCING DC LINK CAPACITOR VOLTAGES

To guarantee proper operation of the CHB converter, voltage of DC link capacitors should always remain close to the reference value [16]. Employing zero energy compensation, net flow of active power between the capacitors and the network would be zero. However, the capacitors and H-bridge cells have internal losses which lead to small discharge currents inside the capacitors and voltage drop.

Transients and measurement errors can also lead to flow of active power. Hence, an active voltage balancing algorithm should be implemented to control the voltage of DC link capacitors. The voltage control scheme, implemented in this research, has two steps: (i) it keeps the total voltage of DC links (VCT) close to the reference value (VCTRef) and (ii) it provides voltage balance among the DC link capacitors. Total DC link voltage is sum of individual DC link voltages, hence

$$v_{CT} = \sum_{i=1}^{6} V_{C_i} \quad (5)$$

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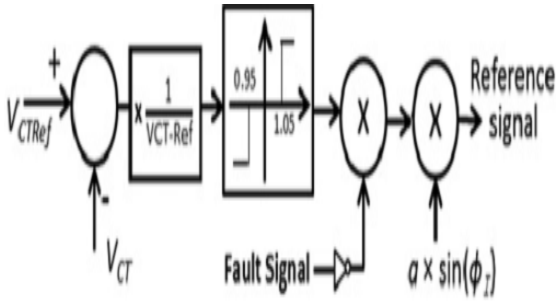
And

$$V_{CRTef} = 6\,V_{CRef} \quad (6)$$

where VCi is DC link voltage of the ith cell. Therefore, performing the two steps of the voltage control scheme guarantees correct regulation of DC link voltages. The first step is performed via two controllers: controller I and controller II, which are displayed in Fig 3.

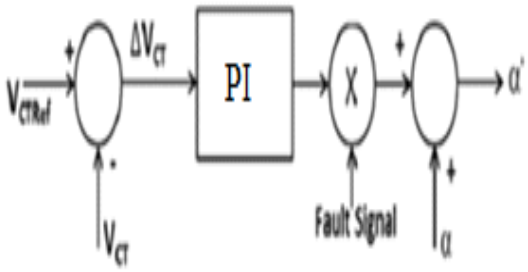
Controller I is active whenever the DVR is in standby mode, and controller II performs the regulation of VCT during compensation period. These controllers keep the total DC link voltage close to the reference value, but cannot maintain voltage balance among DC link voltages. Therefore, a voltage balancing mechanism is also employed to keep the voltage balance, i.e. step 2 of the aforementioned voltage control scheme.



(a)

Fig. 3 Total DC link voltage is controlled by two controllers a) Controller I in standby mode

Controller I is shown in Fig. 3a. It compares VCT with VCTRef and if the difference (ΔVCT) exceeds a predefined margin, it will attempt to bring the DC link voltage, VCT, to the acceptable range. Therefore, controller I is able to control the total DC link voltage when the DVR is in standby mode. Magnitude of the charging/discharging current depends on amplitude of the sinusoidal reference signal. Large charging/discharging current can lead to undesirable voltage drop on the line impedance and filters.



b)

Fig. 3 Total DC link voltage is controlled by two controllers b) Controller II in compensation mode

Fig. 3b displays controller II. This controller is activated during compensation and controls total DC link voltage. During compensation, the voltage signal of the voltage source inverter is perpendicular to line current, preventing exchange of active power between the DVR and the network. However, internal losses could discharge DC link capacitors or cause exchange of small amounts of active power and therefore change the total DC link voltage.

In this scheme, participation of H-bridge cells in synthesizing a voltage level is decided based on two rules: (i) the line current being charging or discharging; and (ii) which cells need to be charged and which ones need to be discharged. Three modes are defined for H-bridge cells: '+1', '0' and 'PWM'. In '+1' mode, the AC terminal voltage of an H-bridge cell is equal to DC link voltage VCRef.

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According to demonstrated flowchart in Fig. 4, at the beginning of each balancing period, this method sorts the H-bridge cells based on their DC link voltages. Operating mode of each cell depends on its rank in the sorting and the voltage level that is to be synthesized.

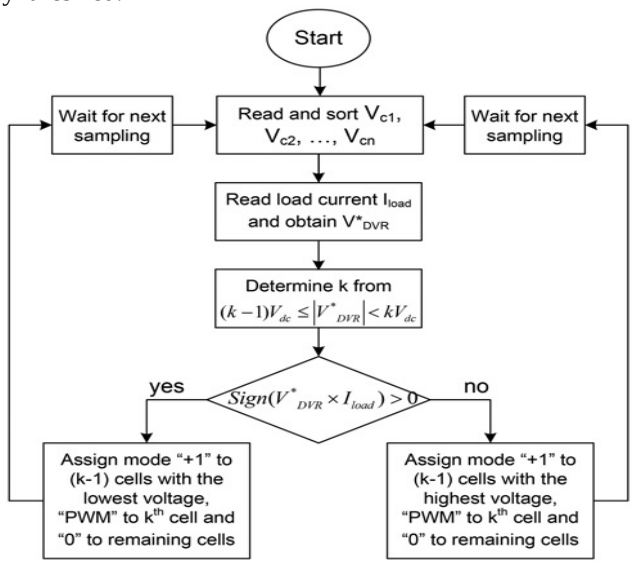

Fig. 4 Flowchart of voltage balancing algorithm in the CHB inverter

In case of charging current, the (k − 1) cells with the lowest voltage, i.e. the ones which need charge are selected to operate in '+1' mode, the kth cell in 'PWM' and the rest in '0' mode. If the current is discharging, the (k − 1) cells with the highest voltage must be discharged by working in '+1' mode, the kth cell in 'PWM' and the rest in '0' mode.

Including the DVR introduced in this paper. Accuracy and settling time delay are the key parameters in assessment of estimation methods. Most applications employ Park transform and fast Fourier transform (FFT) methods for estimation of sinusoidal waveforms. High accuracy and small delay of Park transform are desirable, but it can only estimate balanced three-phase systems. Additionally, its dynamic behavior is highly dependent on behavior of the PLL implemented in it.

For example, to synthesize a voltage between 3VCRef and 4VCRef when the current is charging, three cells with the lowest voltage are selected to operate in '+1' mode, the fourth one in 'PWM' mode and the rest in '0' mode. Using this strategy, not only is the DVR voltage synthesized, but also the DC link capacitors are balanced.

Table 2
DVR performance comparison between previous studies and the current study

study	Converter type	Medium voltage(MV) connection	Energy Storage	Switching frequency	Voltage balance	Unbalanced compensation	Size of line filter	Harmonic mitigation
[7]	2-level	transformer	batteries	high	-	no	medium	no
[8]	2-level	transformer	batteries	high	-	no	medium	yes
[9]	Matrix	transformer	Grid	high	-	no	medium	no
[10]	AC-AC,buck,boost	transformer	Grid	high	-	no	medium	no
[11]	2-level, AC-AC CHB	transformer	Grid	high	-	no	medium	no
[12]	CHB	direct	batteries	low	-	yes	small	yes
[13]	CHB,DC-DC	direct	batteries	low	-	no	small	no
[14]	CHB	direct	Capacitors	low	no	yes	small	no
[15]	CHB	direct	Capacitors	low	yes	yes	small	yes

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IV. ESTIMATION METHOD

Estimation of amplitude and phase of sinusoidal three-phase voltages and currents is an important issue in many PQ applications, including the DVR introduced in this paper. Accuracy and settling time delay are the key parameters in assessment of estimation methods. Most applications employ Park transform and fast Fourier transform (FFT) methods for estimation of sinusoidal waveforms. High accuracy and small delay of Park transform are desirable, but it can only estimate balanced three-phase systems. Additionally, its dynamic behaviour is highly dependent on behaviour of the PLL implemented in it.

However, Park transform is still employed in several applications, including active power filters, electrical machine control and sub-synchronous oscillations

$$\begin{bmatrix} v_q(t) \\ v_d(t) \\ v_z(t) \end{bmatrix} = \frac{2}{3} * \begin{bmatrix} sin(wt) & sin(wt-2\pi/3) & sin(wt+2\pi/3) \\ cos(wt) & cos(wt-2\pi/3) & cos(wt+2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} * \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \quad (7)$$

Vq, Vd and Vz in (7) are D, Q and DC elements of the three-phase system comprised of Va, Vb and Vc, respectively. The estimation method employed for simulation study (in this paper). It uses Park transform and theory of positive, negative and zero sequences. To compare the performance of the proposed multilevel DVR and its control strategy with the previous approaches, a comparison is carried out and is given in Table 2.

V. SIMULATION RESULTS

Three simulation scenarios are defined and performed to assess the performance of the new DVR under different voltage sags. Table 3 lists parameters of the simulation. The network voltage and load are selected similar to the MWPI network.

Table 3
System parameters under simulation study

Network	
Parameter	Value
network voltage	20 kV
load power	35 MW
load power factor	0.78 inductive
CHB converter	
voltage of DC link capacitor	1.33 kV
number of H-bridge cells per phase	6
line filter inductor	1.1 mH
line filter capacitor	90 μF
switching frequency	2 kHz

Three-Phase Voltage Sag

A three-phase balanced voltage sag with depth of 20% occurs at t = 0.2 s and lasts for ten fundamental cycles.

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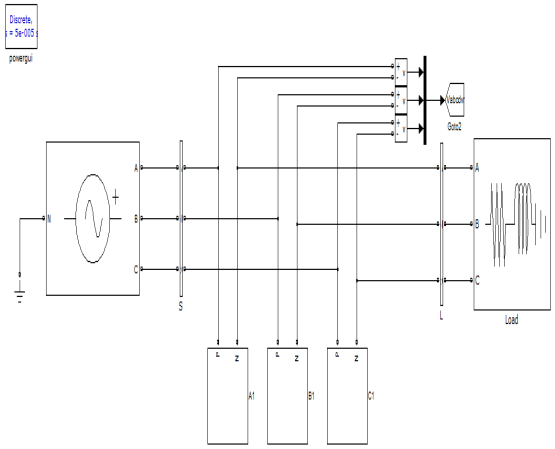

Fig.10 Block diagram of simulation

The voltage balance between individual capacitors is well provided. Additionally, the ripple of DC link voltages is lower than ±10% and the ripple frequency is 2f0; where f0 is the fundamental frequency of the network, i.e. 50 Hz. Therefore, the voltage control scheme is working well.

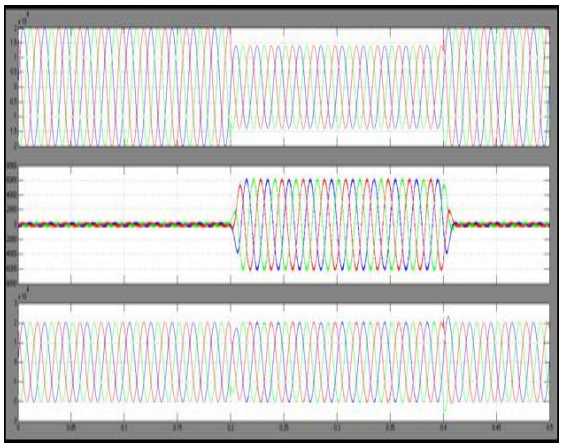

Fig. 11 Three-phase voltage sag a Network voltage b Injected voltage by the DVR c Load-side voltage

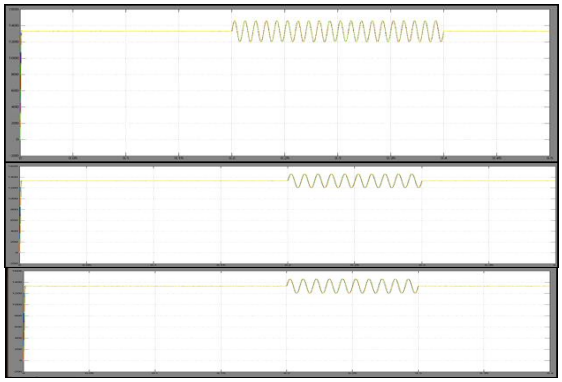

Fig. 13 Voltages of the DC link capacitors

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Single-Phase Voltage Sag

Fig.14 shows the network voltage, DVR voltage and restored supply voltage. It demonstrates that the DVR can successfully distinguish and mitigate unbalanced voltage sags.

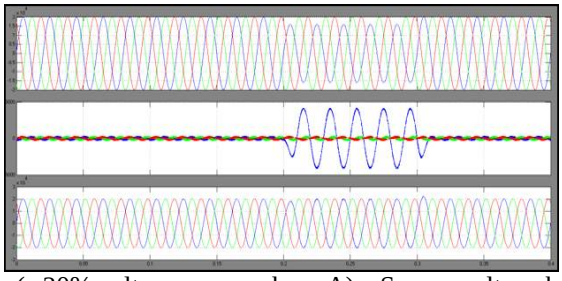

Fig. 14 Unbalanced voltage sag (a 20% voltage sag on phase A) a Source voltage b Injected voltage by the DVR c Load-side voltage

Three-Phase Voltage Sag With Voltage Harmonics

In this simulation, capability of the proposed DVR is assessed in presence of voltage harmonics. Fig.16a shows the network voltage. A three-phase voltage sag with depth of 20% occurs at t = 0.2 s and lasts for five cycles.

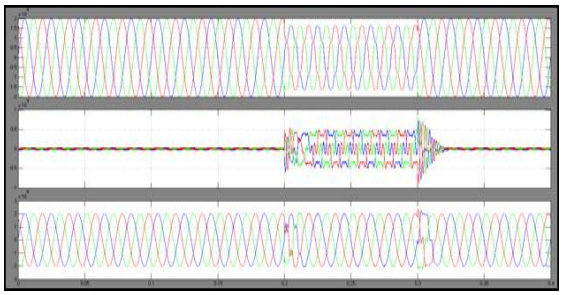

Fig.16 Three-phase 20% voltage sag with voltage harmonics a Network voltage b Injected voltage by the DVR c Load-side voltage

VI.CONCLUSION

In this paper proposes the design and analysis of a dynamic voltage restorer (DVR) which employs a cascaded multilevel inverter with capacitors as energy sources. According to the design and performance assessment of a DVR supported the voltage sag information collected from MWPI is planned during this paper. By utilizing the multilevel convertor, the proposed DVR was capable of direct association to the medium voltage-level network without a series injection electrical device. Because of internal losses of H-bridge cells and probable inaccuracies in measurements, voltage of DC link capacitors might become unequal that prevents proper operation of the convertor. A voltage control scheme, comprised of 3 separate controllers, was planned during this paper for keeping voltage balance among the DC link capacitors inside nominal vary. A system permits for a discount of unsure effects within the system control and improves the efficiency. By utilizing the simulation results we will to verify the performance of CHB-based DVR.

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